RICKY TRAN

COMPUTER ENGINEER · SOFTWARE ENGINEER · ELECTRICAL ENGINEER

Melbourne/Orlando, Florida / Space Coast

☐ (+1) 561-542-6247 | ✉ rickydtran@gmail.com | ⌂ www.rickytran.com | Active TS/SCI Clearance

Skills and Languages

Expertise	FPGA/HDL Design and Verification, Digital System Architecture, Embedded Systems, IoT
Programming	VHDL, Perl, Python, TCL, C/C++, JS, Java
Implementation	Xilinx Vivado, ISE, Altera Quartus, Synopsys Synplify Pro, Microsemi Libero SoC
Simulation	Cadence NCSim/Xcelium, Questasim/Modelsim, Mathworks MATLAB
Verification	Xilinx Chipscope, Real Intent Ascent Lint/Meridian, Mathworks HDL Cosimulation
Version Control	Apache Subversion, GIT, Oracle PDM
Databases	MongoDB, Redis, MySQL, SQLite
Languages	Conversational Vietnamese, Elementary Spanish

Experience

L3Harris Technologies
Palm Bay, Florida
ELECTRIAL ENGINEER, DIGITAL/SIGNAL PROCESSING — *Jan. 2018 - Present*

- Major contributor to F-35 TR3 Program on various FPGA platforms and applications from redevelopment to integration and test support
- Worked on fast pace Tiger Team to redesign and test FPGA architecture of an application in 3 months compared to inital design's 3 year effort
- Designed, verified, and hardware tested custom Flash Controller for Boot Sequencer / Sanitizer
- Developed python lab test environment for multiple FPGA applications that would be eventually pulled into a software Integration and Test framework
- Redesign and verification of custom SPI/QSPI Interfaces
- Created multiple new robust build environments for Xilinx, Altera, and Microsemi FPGAs
- Designed, verified, and hardware tested FPGA based Ethernet Packet Generator Checker used for BIT testing
- Reachitectured and design of middleman FPGA application with 10G switching/passthrough, PCIE, etc. capabilities
- Contributed and designed of blocks for FPGA-based Deep Learning Convolutional Neural-Net Application
- Designed, verified, and tested FPGA implementation of a Min-Max Heap/Priority Queue
- Majorly contributed to a Common Development Environment, a core group of scripts used to reduce risk and improve productivity of FPGA development. This eventually became the defacto standard environment for FPGA design
- Served as lead for a Camera Display Bridge Application to create a video stream over the air used to demonstrate capabilities of a in-house Software Defined Radio
- Performed multiple formal FPGA Application Requirements Sell-Offs and Close Outs for Quality and Mission Assurance
- Designed, verified, and hardware tested COMSEC key storage interface with Single Error Correction and Double Error Detection
- Designed and architected flow control for High Data Rate Modulator capable of 2 Gbps fora Small-Satellite platform
- Designed, verified, and hardware tested baseband processing blocks for Frame Header Encoding with Unique Word insertion and Frame Payload Generation
- Digital design and integration and test experience on Aerospace Applications and Digital Payloads and Platforms
- Supported new graduate recruiting efforts by performing phone interviews and attended panels

Flow Development and Technology
Philidelphia, Pennsylvania
INDEPENDENT CONSULTANT/HARDWARE/SOFTWARE ENGINEER — *Jan. 2019 - Oct. 2020*

- Architected scalable backend software and hardware architecture for proprietary smart commercial building platform
- Developed embedded code to interface with proprietary biometric access solutions for preliminary design / prototype
- Provided oversight and lead team of software developers to create an end to end solution

Harris Corporation
Palm Bay, Florida
ELECTRIAL ENGINEER INTERN — *May. 2017 - Aug. 2017*

- Designed multiple GUI-based tools in MATLAB to automate data collection and tool setup for anechonic chamber testing
- Exposure to theory and application of spread-spectrum techniques and chaotic signal processing
- Low Probability of Detection/Interception (LPD/LPI) Digital Communications
- Designed FPGA implementation of rate-line detector in VHDL
- Exposure to ground-up development of high-rate, real-time signal processing algorithms in hardware (FPGA)

Integrated Product and Process Design Program (IPPD)
Gainesville, Florida
COMPUTER ENGINEER LEAD — *Aug. 2016 - May 2017*

- Developed Bluetooth/Wi-Fi IoT user management tracking system to improve effcency in construction industry
- Implemented backend API for client and hardware communication
- Developed code for ESP8266 microcontrollers to successfully act as sensor nodes and communicate over Wi-Fi to server via MQTT
- Integrated and interfaced HC05 bluetooth module with ESP8266 codebase and interact over a serial communication
- Worked in a multidisciplinary design team and exposure to business disciplinary skills on design projects

NSF Center for High Performance Reconfigurable Computing (CHREC) *Gainesville, Florida*
Undergraduate Research Volunteer (F6 Group) *Jun. 2016 - Dec. 2016*
- Exposure to implementation and testing on Texas Instruments Keystone 2 Digital Signal Processor
- Developed Single-Precison Finite Impulse Response Filter(SPFIR) with L2 cache optimzation utilizing a ping-pong DMA transfer scheme
- Learned OpenCL and OpenMP frameworks and analyzed existing code for existing filters
- Ran benchmarks and deciphered metrics to evaluate performance

Extracurricular Activity

Gator Engineering @ Santa Fe Program (GE@SF) *Gainesville, Florida*
Ambassador *Jan. 2014 - Present*
- First cohort of first of its kind program aimed towards alleviating filled critical tracking courses in engineering
- Communicated and advised with prospective students that showed interest towards the program
- Conducted campus tours of the Herbert Wertheim College of Engineering

Gator Robotics Club (Tailgator 2.0) *Gainesville, Florida*
Computer Engineer *Sep. 2014 - May 2016*
- Autonomous burger-grilling drink dispenser
- Refined a personal proximity sensor to work with project specs
- Developed overall grill code, complete overhaul from previous iterations
- Mentor to prospective students interested in learning more about robotics

Honors

2021	**Technology Innovation Award**, L3Harris Technology and Engineering Awards	*Palm Bay, Florida*
2017	**Acknowledgement**, Investigating TI KeyStone II and Quad-Core ARM Cortex-A53 Architectures for On-Board Space Processing	*Pittsburgh, Pennsylvania*

Education

University of Florida *Gainesville, Florida*
Master of Business Administration *Anticipated May 2024*

University of Florida *Gainesville, Florida*
Master of Science in Industrial and Systems Engineering *Anticipated May 2023*

University of Florida *Gainesville, Florida*
Bachelor of Science in Computer Engineering *December 2017*
- GPA: 3.29/4.00
- Coursework: Reconfigurable Computing, Computer Architecture, Operating Systems, Digital Design, Advanced System Programming, IPPD 1+2, Introduction to Software Engineering, Concurrent Programming, Microprocessor Applications, Digital Logic and Computer Systems, Data Structures and Algorithms, Introduction to Signals and Systems, Circuits 1, Applications of Discrete Structures, Programming Fundamentals 1+2